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APPLICATION NO	). F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,847		12/10/2001	Theodore J. Letavic	US 010610	3619
24737	7590	05/14/2003			
PHILIPS ELECTRONICS NORTH AMERICAN CORP 580 WHITE PLAINS RD TARRYTOWN, NY 10591				EXAMINER LEWIS, MONICA	
				2822	
				DATE MAILED: 05/14/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. Applicant(s 10/015,847 LETAVIC ET AL. Office Action Summary Examiner **Art Unit** Monica Lewis 2822 -- The MAILING DATE of this communication appears on the cov r sheet with the correspondenc address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). **Status** 1) 🖂 Responsive to communication(s) filed on 05 March 2003. 2a)⊠ This action is FINAL. 2b) This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. **Disposition of Claims** 4) Claim(s) 1-12 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) \_\_\_\_\_ is/are allowed. 6) Claim(s) 1-12 is/are rejected. 7) Claim(s) \_\_\_\_\_ is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. **Application Papers** 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) ☑ The proposed drawing correction filed on <u>05 March 2003</u> is: a) ☑ approved b) ☐ disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action. 12) The oath or declaration is objected to by the Examiner. Priority under 35 U.S.C. §§ 119 and 120 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some \* c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). \* See the attached detailed Office action for a list of the certified copies not received. 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application). a) The translation of the foreign language provisional application has been received. 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. Attachment(s)

U.S. Patent and Trademark Office PTO-326 (Rev. 04-01)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)

Interview Summary (PTO-413) Paper No(s).

Notice of Informal Patent Application (PTO-152)

## **DETAILED ACTION**

1. This action is in response to the amendment filed March 5, 2003.

## Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-5, 7-9 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art.

In regards to claim 1, Merchant discloses the following:

- a) a buried oxide layer (2) formed over a semiconductor substrate (3) (For Example: See Figure 1);
- b) a silicon layer (1) formed over the buried oxide layer (For Example: See Figure 1);
- c) a top oxide layer (6) formed over the silicon layer (For Example: See Figure 1); and
- d) a first gate oxide (8) formed over the silicon layer adjacent the top oxide layer (For Example: See Figure 1).

In regards to claim 1, Merchant fails to disclose the following:

a) a second gate oxide formed over a portion of the first gate oxide.

However, Applicant's Related Art discloses a second gate oxide over a portion of the first gate oxide (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to

Application/Control Number: 10/015,847

Art Unit: 2822

include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

In regards to claim 2, Merchant discloses the following:

a) the silicon layer comprises a source region (10), a body region (9), and a drift region (4) (For Example: See Figure 1).

In regards to claim 3, Merchant discloses the following:

a) the first gate oxide is formed over the drift region, the body region, and the source region (For Example: See Figure 1).

In regards to claim 4, Merchant discloses the following:

a) the first gate oxide, top oxide layer and the body region (For Example: See Figure 1).

In regards to claim 4, Merchant fails to disclose the following:

a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

Art Unit: 2822

In regards to claims 5 and 9, Merchant discloses the following:

a) a field plate (7) formed over the top oxide layer, the first gate oxide (For Example: See Figure 1).

In regards to claims 5 and 9, Merchant fails to disclose the following:

a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing the breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

In regards to claims 7 and 11, Merchant fails to disclose the following:

a) the first gate oxide has a length of approximately 3-4um, and wherein the second gate oxide has a length of approximately 1-2um.

However, the applicant has not established the critical nature of the dimension where the first gate oxide has a length of approximately 3-4*u*m, and wherein the second gate oxide has a length of approximately 1-2*u*m. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Application/Control Number: 10/015,847 Page 5

Art Unit: 2822

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In regards to claim 8, Merchant discloses the following:

a) a buried oxide layer formed over a semiconductor substrate (For Example: See Figure 1);

b) a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region (For Example: See Figure 1);

c) a top oxide layer formed over the silicon layer (For Example: See Figure 1); and

d) a first gate oxide formed over the silicon layer adjacent the top oxide layer (For Example: See Figure 1).

In regards to claim 8, Merchant discloses the following:

a) the first gate oxide, top oxide layer and the body region (For Example: See Figure 1).

In regards to claim 8, Merchant fails to disclose the following:

a) a second gate oxide.

However, Applicant's Related Art discloses a second gate oxide (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a second gate oxide as disclosed in Applicant's Related Art because it aids in increasing breakdown voltage.

Additionally, since Merchant and Applicant's Related Art are both from the same field of endeavor, the purpose disclosed by Applicant's Related Art would have been recognized in the pertinent art of Merchant.

Art Unit: 2822

4. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art and Seeds et al. (U.S. Patent No. 3,936,858).

In regards to claims 6 and 10, Merchant discloses the following:

a) the first gate oxide has a thickness in a range of approximately 300-600A (For Example: See Column 2 Lines 39 and 40).

In regards to claims 6 and 10, Merchant fails to disclose the following:

a) a second gate oxide has a thickness in a range of approximately 900-1200A.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (For Example: See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness around 1200A as disclosed in Seeds because it aids in increasing the threshold voltage.

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Finally, since Merchant and Seeds are both from the same field of endeavor, the purpose disclosed by Seeds would have been recognized in the pertinent art of Merchant.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Applicant's Related Art, Seeds et al. (U.S. Patent No. 3,936,858) and Shirahata et al. (U.S. Publication No. 2002/0175380).

Page 7

In regards to claim 12, Merchant fails to disclose the following:

a) a thickness of approximately 1200A of the second gate oxide results in an increase from approximately 1e<sup>12</sup>cm<sup>-2</sup> to approximately 2e<sup>12</sup> cm<sup>-2</sup> of a maximum allowable charge, and a decrease of approximately 30% for a specific-on-resistance of the device.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (For Example: See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness in a range of approximately around 1200A as disclosed in Seeds because it aids in increasing the threshold voltage.

However, Shirahata et al. ("Shirahata") discloses a gate oxide that has various charges (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a various charges as disclosed in Shirahata because it aids in increasing the threshold voltage.

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected

Page 8

Art Unit: 2822

results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Finally, since Merchant, Seeds and Shirahata are both from the same field of endeavor, the purpose disclosed by Seeds and Shirahata would have been recognized in the pertinent art of Merchant.

## Response to Arguments

6. Applicant's arguments filed March 5, 2003 have been fully considered but they are not persuasive. Applicant argues that the "Office has misinterpreted Applicant's Related Art, and that the cited combination of references fail to teach or suggest a second gate oxide formed over a portion of the first gate oxide." However, Applicant's Prior Art does disclose a second gate oxide formed over a first oxide (For Example: See Figure 2). The Examiner has attached marked up figures of the prior art and present invention to illustrate where the gate oxides are located (For Example: See Figure 2, Figure 3 and Column 6 Lines 12-23 and Column 7 Lines 1-2).

Therefore, Applicant's arguments are not persuasive.

#### Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

Application/Control Number: 10/015,847

Art Unit: 2822

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

8. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Monica Lewis whose telephone number is 703-305-3743.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir

Zarabian can be reached on 703-308-4905. The fax phone number for the organization where

this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

May 6, 2003

AMIR ZARABIAN
PERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Page 9

IOCKSHV. OHILOE

INVENTOR: MARK SIMPSON ET AL
Attorney Docket: US 010610
CH-VOLTAGE SEMICONDUCTOR DEVICE AND METHE OR FORMING THE SAME
Contact: STEVEN R. BIREN 914) 333-9630

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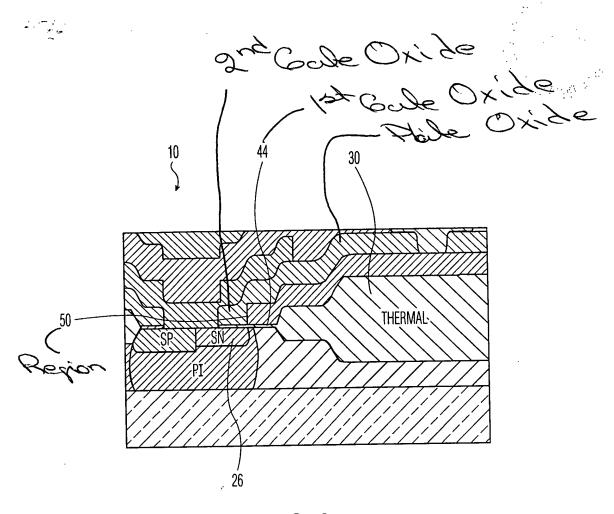


FIG. 2 **RELATED ART** 

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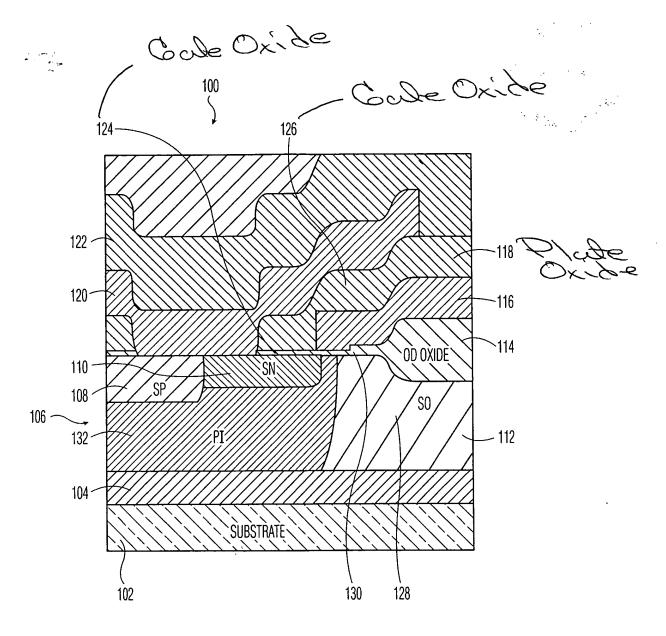


FIG. 3